IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

On page 7, please replace paragraph [0029] with the following amended paragraph:

[0029] The SA is then sent to the BS 104 over a channel on the reverse link [[108b]] 108B. In one embodiment of the invention, the reverse link channel is a DRC.

On page 8, please replace paragraph [0034] with the following amended paragraph:

[0034] FIG. 2 shows the forward link signal structure transmitted by each base station in an exemplary high data rate system. Forward link signals are divided into fixed-duration time slots. In an exemplary embodiment, each time slot is 1.67 milliseconds long. Each slot 202 is divided into two half-slots 204, with a pilot burst 208 transmitted within each half-slot 204. In an exemplary embodiment, each slot is 2048 chips long, corresponding to a 1.67 millisecond slot duration. In an exemplary embodiment, each pilot burst 208 is 96 chips long, and is centered at the mid-point of its associated half-slot 204. A reverse link power control (RPC) signal 206 is transmitted to either side of the pilot burst in every second half-slot [[204b]] 204B. In an exemplary embodiment, the RPC signal is transmitted in the 64 chips immediately before and the 64 chips immediately after the second pilot burst [[208b]] 208B of each slot 202, and is used to regulate the power of the reverse link signals transmitted by each subscriber station. In an exemplary embodiment, forward link traffic channel data are sent in the remaining portions of the first half-slot 210 and the remaining portions of the second half-slot 212. In an exemplary embodiment, preamble 214 is 64 chips long and is transmitted with each packet. Because the traffic channel stream is intended for a particular MS, the preamble is MS specific.

On page 9, please replace paragraph [0039] with the following amended paragraph:

[0039] If the payload unit is to be retransmitted, the method continues in step 306, in which the payload unit is provided to a ~~first-time~~ retransmission queue.

On page 12, please replace paragraph [0058] with the following amended paragraph:

[0058] The packets arriving at the MS 106 over the forward link [[108a]] 108A are provided to a preamble detector 520, which detects and decodes a preamble of the packets. The preamble is provided to a processor 521, which compares the decoded preamble to a reference preamble. The packet is discarded if the preamble indicates that the packet is intended for another MS; otherwise, the packet is provided to a decoder 522, which decodes the packet. The decoded packet is provided to a processor 521, which evaluates a quality metric of the packet. The evaluated quality metric and the quality metric contained in the received packet are compared, and based on the comparison, an SA generator 526 generates an appropriate SA. Though the preamble detector 520, the decoder 522, and the processor 521 are shown as separate elements, one skilled in the art will appreciate that the physical distinction is made for explanatory purposes only. The preamble detector 520, the decoder 522, and the processor 521 may be incorporated into, single processor accomplishing the above-mentioned processing.

On page 13, please replace paragraph [0061] with the following amended paragraph:

[0061] The RLP processor 526 checks the sequence numbers of the delivered payload units. If the sequence number indicates contiguity, the RLP processor 524 delivers data from the buffer 528 to the data sink 534. Otherwise, the RLP processor 526 instructs RLP message generator 532 to generate RLP message requesting retransmission of the missing units. In one embodiment of the invention, the RLP message requests retransmission of all of the missing units in the buffer 528. In another embodiment, the message requests retransmission of only the latest detected missing payload units. The message is then transmitted over the reverse link [[108b]] 108B to the BS 104.

On page 14, please replace paragraph [0066] with the following amended paragraph:

[0066] FIG. 6 illustrates a relationship between a packet received at a MS 106 and a SA transmitted from the MS 106. In slots n-4, n-3, a receiver at the MS 106 receives a packet over the forward channel link [[108a]] 108A, and determines if the packet was intended for the MS 106. The MS 106 discards the packet if the packet was not intended for the MS 106. Otherwise, the MS 106 decodes the packet, evaluates a quality metric of the packet, and compares the

evaluated quality metric with the quality metric contained in the packet in slots n-2, n-1. In slot n, a transmitter at the MS 106 sends a SA back to the BS 104 over the reverse channel link [[108b]] 108B. In slot n+1, the SA received at the BS 104 is decoded and provided to a QARQ controller. In slots n+2, n+3 the BS 104 retransmits the packet if so requested. The position of the slots on the received forward link channel [[108a]] 108A and the reverse link channel [[108b]] 108B is synchronized at the MS 106. Therefore, the relative position of slots on the forward channel link [[108a]] 108A and the reverse channel link [[108b]] 108B is fixed. The BS 104 can measure a round trip delay between the BS 104 and the MS 106. Consequently, the time slot in which the SA must arrive at the BS 104 can be ascertained, provided that a relation between the received packet processing and the SA is determinable.